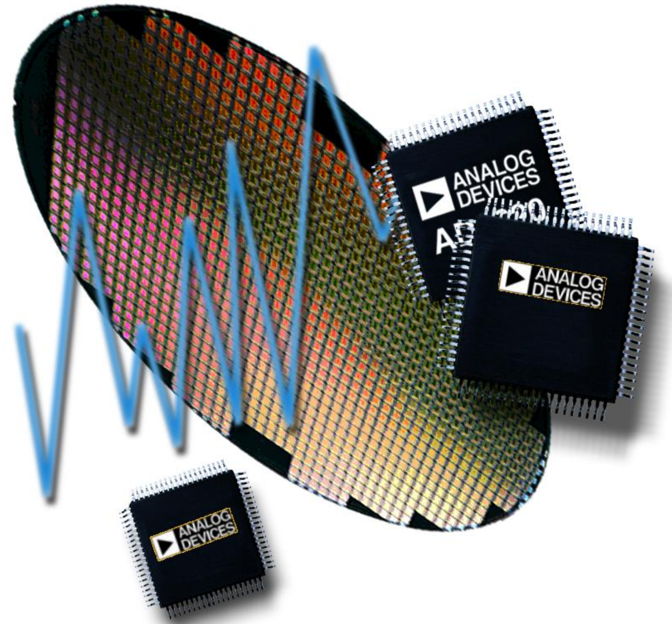

Reliability Report

Report Title: 23x23mm PBGA at AEG Qualification

Report Number: 20196

Revision: A

Date: 14 June 2023

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADSP-21061L product in a 225-BGA package at ASE-AEG. The ADSP-21061L is a 32-bit processor optimized for high performance DSP applications. Table 1 and 3 provides the ADSP-21061L product characteristics.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.5um CMOS

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADSP-21061L
Die Id	TM4092 C-T6
Die Size (mm)	10.33 x 10.54
Wafer Fabrication Site	TSMC Fab-3
Wafer Fabrication Process	0.5um CMOS
Die Substrate	Si
Metallization / # Layers	AlCu(0.5%)/2
Polyimide	Yes
Passivation	undoped-oxide/SiN

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 225-BGA at ASE (AEG)

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADSP-21061L
Package	225-BGA
Body Size (mm)	23.00 x 23.00 x 1.80
Assembly Location	ASE (AEG)
MSL/Peak Reflow Temperature(°C)	3 / 260°C
Mold Compound	Hitachi CEL9750ZHF10AK
Die Attach/Underfill/TIM	Ablestik 2100AC conductive
Terminal Finish Composition	96.5Sn_3.0Ag_0.5Cu
Wire Bond Material/Diameter (mils)	4N Gold / 1.20

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - BGA at ASE (AEG)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
High Temperature Storage Life (HTSL)[1]	JESD22-A103	150°C, 1,000 Hours	ADSP-21061L	Q20196.1.HS1	0/32
Solder Heat Resistance (SHR)[1]	J-STD-020	MSL-3	ADSP-21061L	Q20196.1.SH1	0/11
				Q20196.2.SH2	0/11
				Q20196.3.SH3	0/11
Temperature Cycling (TC)[1,2]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	ADSP-21061L	Q20196.1.TC1	0/32
				Q20196.2.TC2	0/32
				Q20196.3.TC3	0/32
Unbiased HAST (UHST)[1,2]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADSP-21061L	Q20196.1.UH1	0/32
				Q20196.2.UH2	0/32
				Q20196.3.UH3	0/32

[1] Electrical test was performed at Cold temperature.

[2] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	ADSP-21061L	225-BGA	JS-002	1Ω, Cpkg	±750V	C2b

Approvals

Reliability Engineer: Lucille Jordan